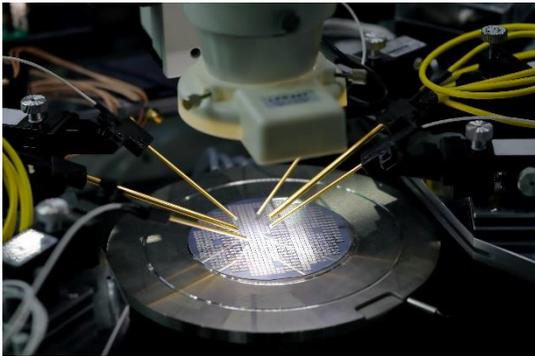


Optimized chip tests

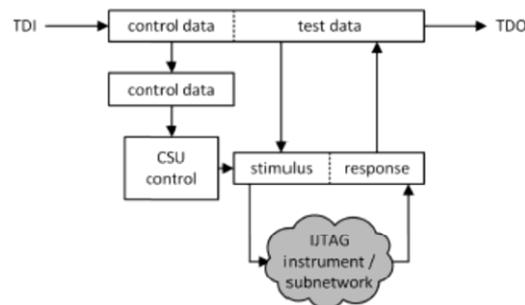
Reconfigurable test structures for fast IC tests

Invention

Integrated circuits, or ICs, must be tested – that is the only way to ensure the required functionality. To this end, test structures are added to circuits. They consist of a test data input (TDI) and a test data output (TDO). Conventional test structures apply a test signal to the test data input and route it through all structures. Normally, only one test data input is available, since space is limited. So tests take a long time and are therefore expensive. For safety reasons, many applications require IC self-tests to be performed during operation. Such in-field tests are described in IEEE1687.



Wafer test, © istock – genkur



Representation of the reconfigurable test structure principles

Current Status

The invention has not yet been implemented in hardware, but fundamental technical feasibility was documented as part of a North Rhine-Westphalia patent validation project. The German patent was granted by the German Patent and Trade Mark Office (DE 10 2017 216 444.1). A European patent application (EP 18 769 698.4) and a U.S. patent application (US 16/616,161) have been disclosed. We are offering interested companies the opportunity to license and refine the technology in collaboration with the inventors and Hamm-Lippstadt University of Applied Sciences.

Relevant Publications

Concurrent IJTAG. Rene Krenz-Baath; Hochschule Hamm-Lippstadt, Workshop Test und Zuverlässigkeit (TuZ'18), 2018

An invention of the Hamm-Lippstadt University of Applied Sciences.

Competitive Advantages

- Time savings
- IC test cost reduction
- Easy to integrate into test processes

Technology Readiness Level

123456789

Technology validated in lab

Industries

- Electrical engineering
- Semiconductor manufacturers

Ref. No.

4991

Contact

Martin van Ackeren

E-Mail: ma@provendis.info

Phone: +49(0)208-94105-34

