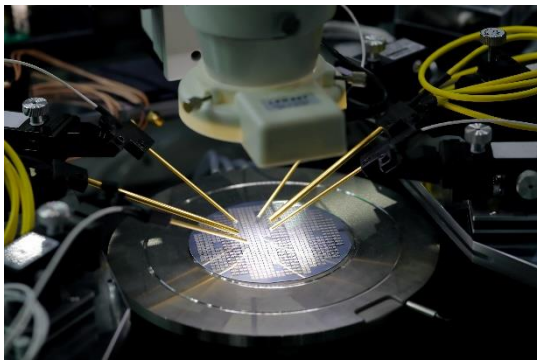
Optimized chip tests

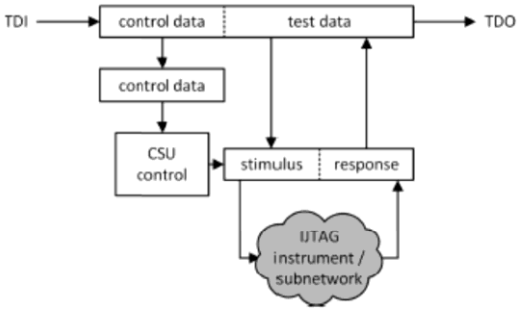
Reconfigurable test structures for fast IC tests

Invention

Integrated circuits, or ICs, must be tested – that is the only way to ensure the required functionality. To this end, test structures are added to circuits. They consist of a test data input (TDI) and a test data output (TDO). Conventional test structures apply a test signal to the test data input and route it through all structures. Normally, only one test data input is available, since space is limited. So tests take a long time and are therefore expensive. For safety reasons, many applications require IC self-tests to be performed during operation. Such in-field tests are described in ISO 26262.



Wafer test, © istock – genkur



Representation of the reconfigurable test structure principles

The new procedure from the Hamm-Lippstadt University of Applied Sciences offers an efficient solution to this problem: It uses a number of reconfigurable test structures connected with intermediate storage. This allows the tests to be performed concurrently, greatly speeding the test process. The intermediate storage and corresponding individual control units are key here. Test data is compressed to further enhance efficiency.

Commercial Opportunities

Although chip producers already invest a great deal of time and money in IC testing, errors often remain undetected because of insufficient test coverage. And large amounts of test data are generated, requiring a great deal of analysis effort. This entails high costs for microchip manufacturers. The new procedure reduces the test time and chip surface required.

Current Status

The invention has not yet been implemented in hardware, but fundamental technical feasibility was documented as part of a North Rhine-Westphalia patent validation project. The German patent was granted by the German Patent and Trade Mark Office (DE 10 2017 216 444.1). A European patent application (EP 18 769 698.4) and a U.S. patent application (US 16/616,161) have been disclosed. We are offering interested companies the opportunity to license and refine the technology in collaboration with the inventors and Hamm-Lippstadt University of Applied Sciences.

Relevant Publications

Concurrent IJTAG. Rene Krenz-Baath; Hochschule Hamm-Lippstadt, Workshop Test und Zuverlässigkeit (TuZ‘18), 2018

An invention of the Hamm-Lippstadt University of Applied Sciences.

Competitive Advantages

- Time savings
- IC test cost reduction
- Easy to integrate into test processes

Technology Readiness Level

1 2 3 4 5 6 7 8 9

Technology validated in lab

Industries

- Electrical engineering
- Semiconductor manufacturers

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